FINAL EXAM (30 POINTS)

*(DUE BY DEC 13th, 2023, 11:59PM PST)*

1. What is Inter-Symbol Interference (ISI)? What are the causes for ISI? What are the effects of ISI on Signal Integrity? How to mitigate ISI?
2. What is common signal in differential pair? How is it generated? What happens if there is a change in common signal? How to reduce common signal changes and its effects in a PCB?
3. What is the target impedance of a Power Distribution Network (PDN)? Why do we need to keep the PDN impedance below target impedance? Why would PDN impedance change with frequency? What determines the maximum frequency for PDN impedance to be controlled?
4. What is parallel resonant frequency (PRF)? How is it generated? What are the effects of having PRF? What are the different ways to reduce the resonant peak at PRF?
5. How does the capacitor brigade work in the PDN? Describe the flow of current from the IC chip to the power supply.
6. What is ground bounce? What are the effects of ground bounce? How to minimize ground bounce?
7. What is skew? How skew can be generated in a differential pair? What are the effects of skew on Signal Integrity? How can the skew be reduced?
8. Why is near-end cross talk always positive? How long does near-end crosstalk last? At what time, the far-end crosstalk can be measured? What is the width of the far-end cross talk?
9. How does ESL of a capacitor affect the PDN impedance? Why is it important to reduce ESL? What are the various types of SMT capacitors that have lower ESL?
10. How does embedded capacitor laminate help in Power Integrity? What are the important design parameters of embedded capacitor laminates? What is the optimal location of embedded capacitor laminates in a PCB, in terms of reducing spreading inductance?